Digital Circuits

ECS 371

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Lecture 10

Office Hours:
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Monday 9:00-10:30, 1:30-3:30
Tuesday 10:30-11:30

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Announcement

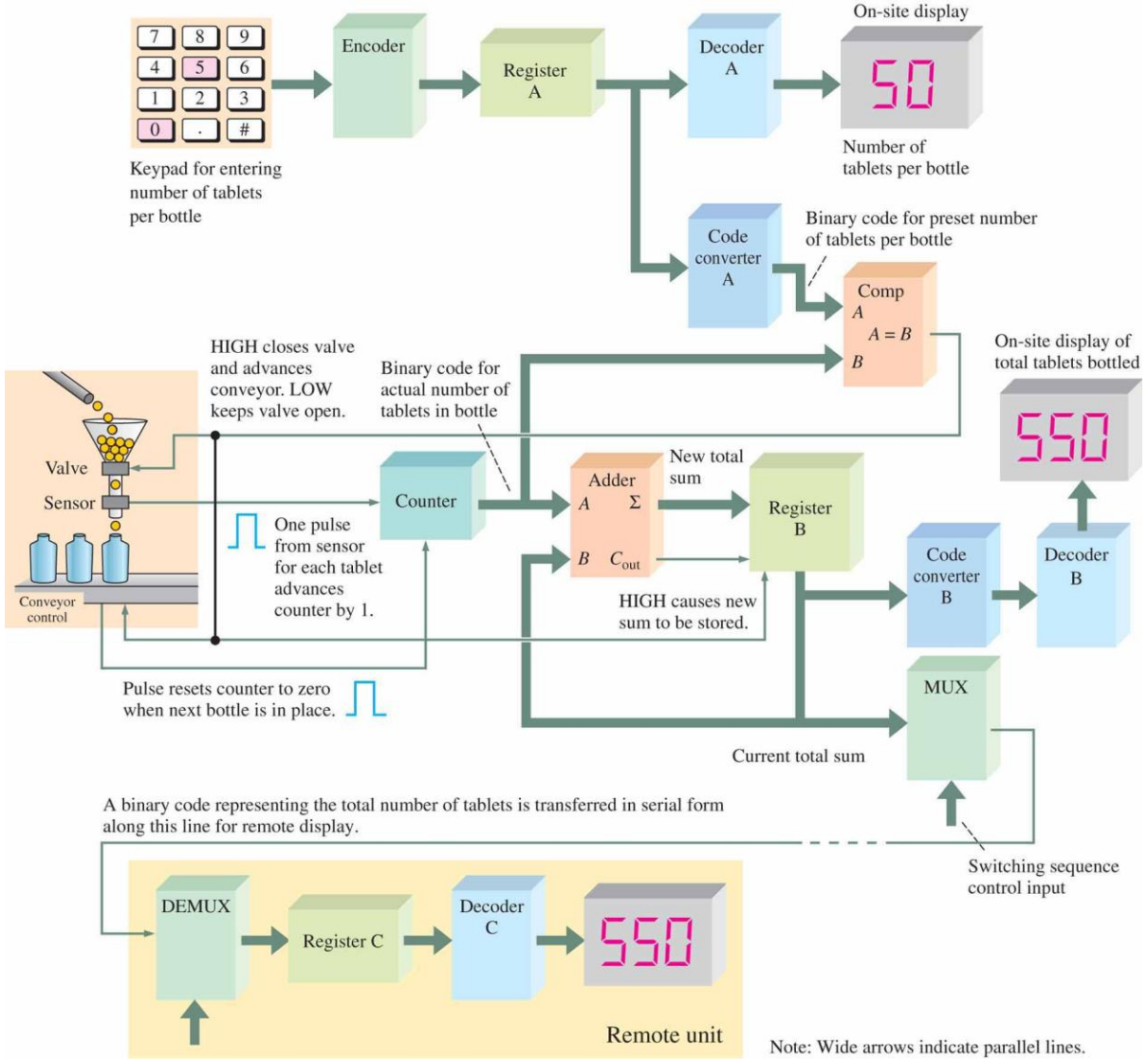
- HW4 posted on the course web site
  - Chapter 5: 4(b,c,e), 20a, 22a, 56
  - **Write down all the steps** that you have done to obtain your answers.
  - Due date: July 16, 2009 (Thursday)

Combinational Logic

- We studied the **theoretical** principles used in combinational logic design.
- We will build on that foundation and describe many of the devices, structures, and methods used by engineers to solve **practical** digital design problems.
- A complex circuit or system is conceived as a collection of smaller subsystems, each of which has a much simpler description.

Digital System Concept

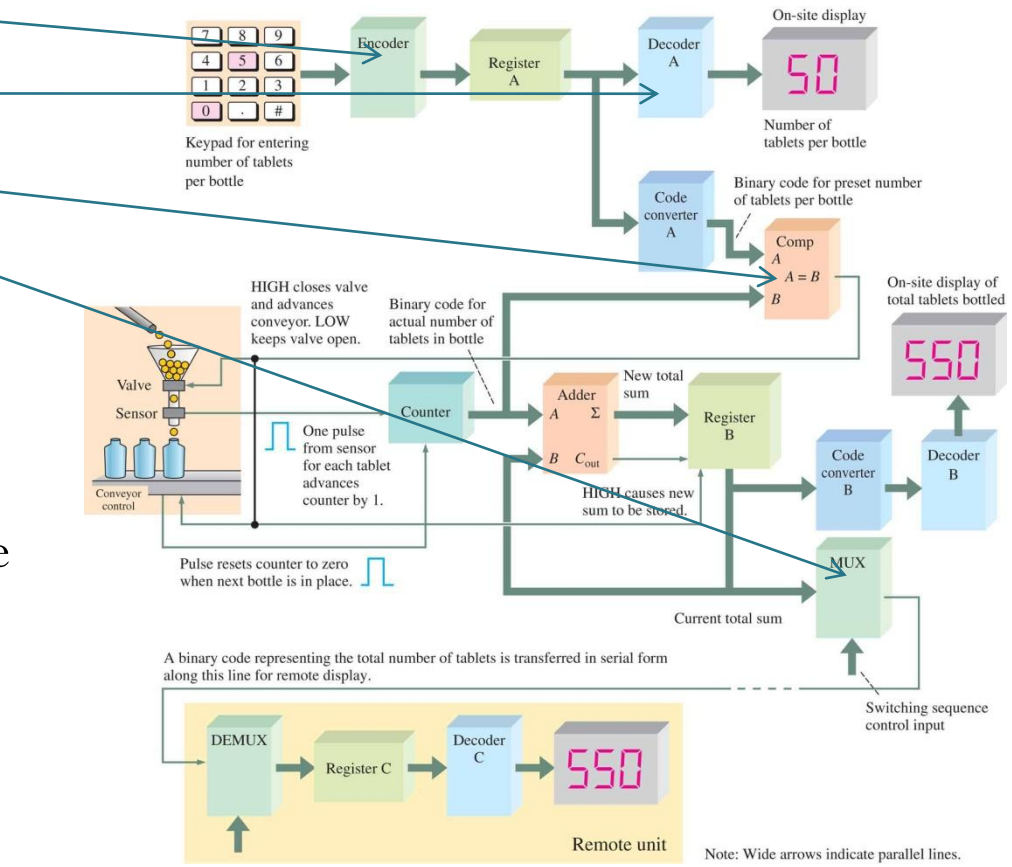
A **digital system** is an arrangement of the individual logic functions connected to perform a specified operation or produce a defined output.



Combinational Building Blocks

- There are several straightforward structures that turn up quite regularly as building blocks in larger systems.
  - Encoder
  - Decoders
  - Comparators
  - Multiplexers

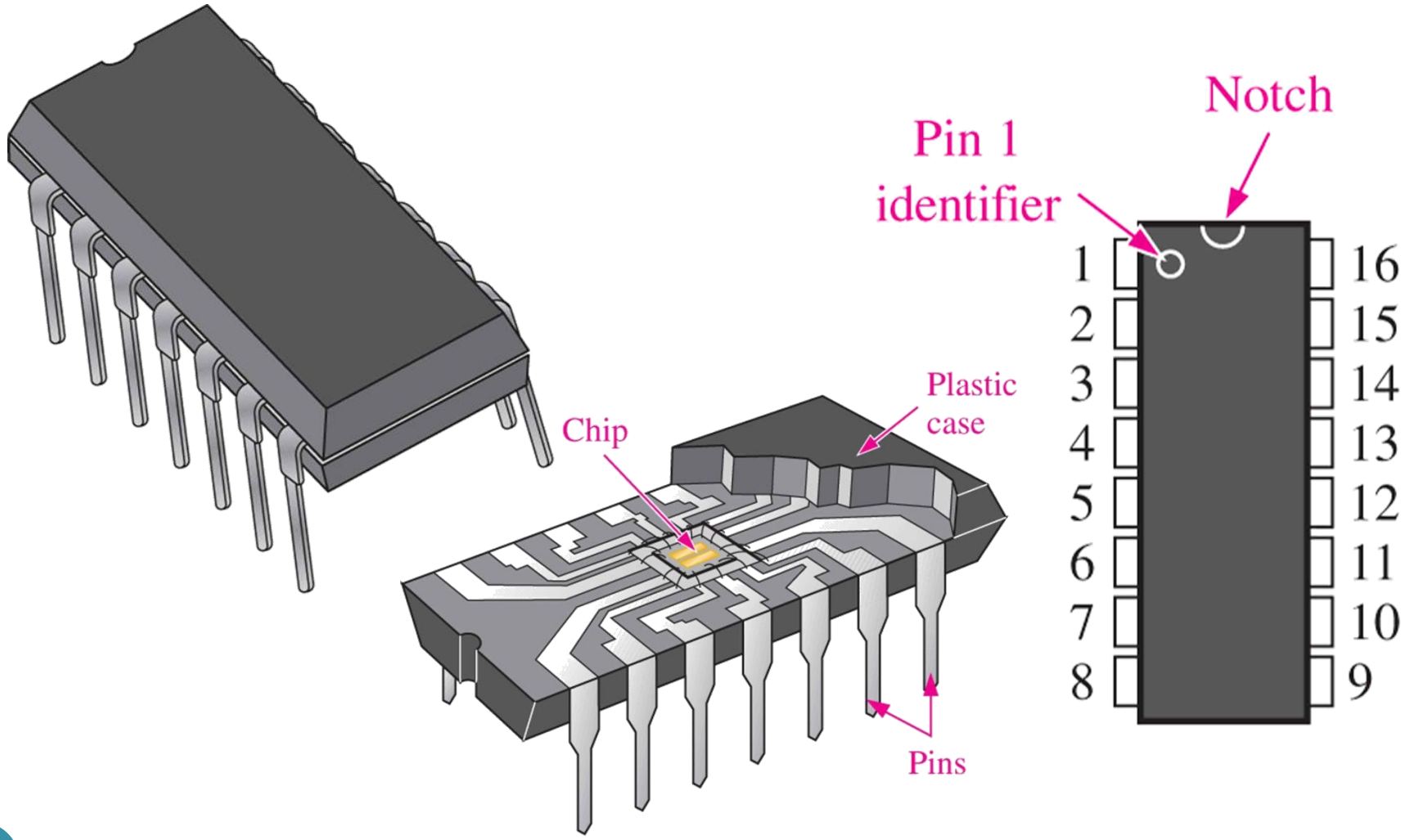
Where can we find these building blocks?



Fixed-function IC

- An integrated circuit (IC) is an electronic circuit that is constructed entirely on a single small chip of silicon.
- Two broad categories of digital ICs.
  1. Fixed-function logic
  2. Programmable logic
- In **fixed-function logic**, the logic functions are set by the manufacturer and cannot be changed.

Fixed-function IC package



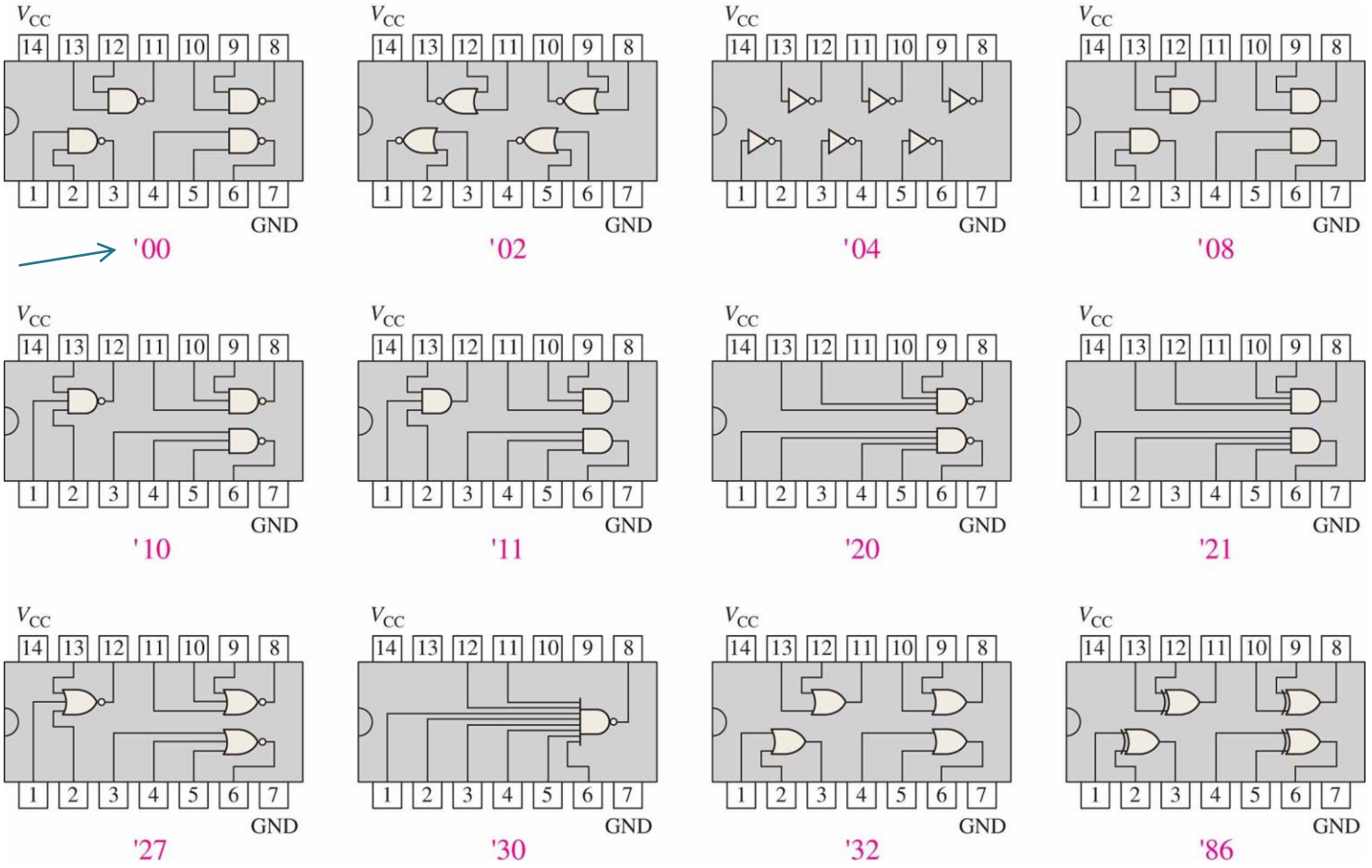
Cutaway view of DIP (Dual-In-line Pins) chip

Complexity Classifications

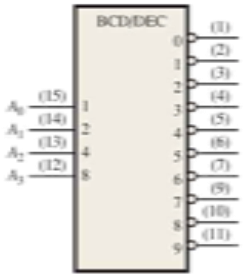
Fixed-function digital lCs are classified according to their complexity.

- **Small-scale integration (SSI)**
  - up to ten equivalent gate circuits on a single chip
  - basic gates and flip-flops.
- **Medium-scale integration (MSI)**
  - from 10 to 100 equivalent gates on a chip.
  - encoders, decoders, counters, registers, multiplexers, arithmetic circuits, small memories
- Large-scale integration (LSI)
- Very large-scale integration (VLSI)
- Ultra large-scale integration (ULSI)

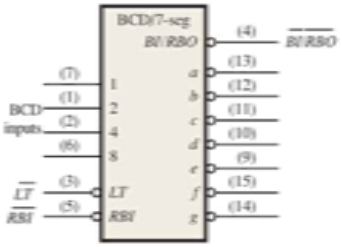
SSI



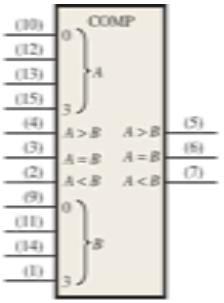
MSI



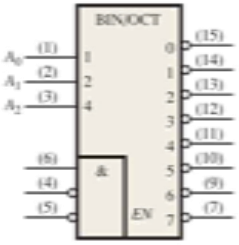
74HC42
BCD-to-decimal decoder



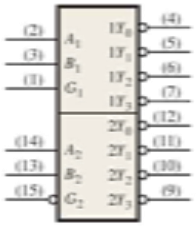
74LS47
BCD-to-7-segment decoder/driver



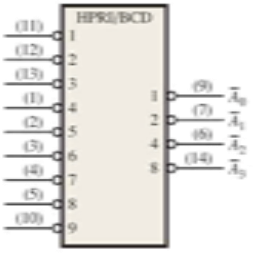
74LS85
4-bit magnitude comparator



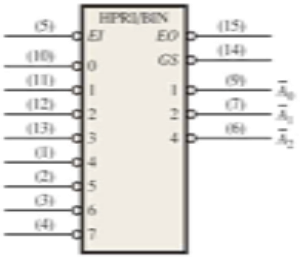
74LS138
3-line-to-8-line decoder



74LS139
Dual 2-line-to-4-line decoder

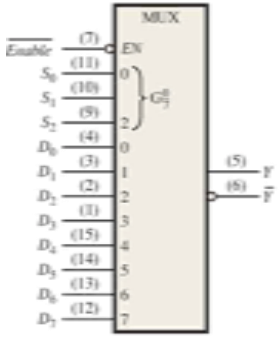


74HC147
Decimal-to-BCD priority encoder

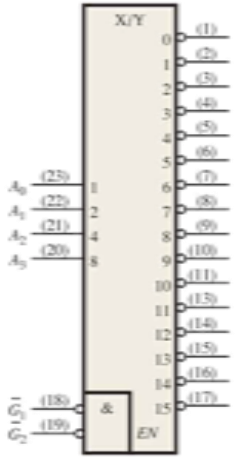


74LS148
Octal-to-binary encoder

For the next couple lectures, we will study most of these 74-series MSI.

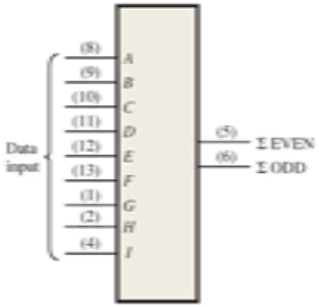


74LS151
8-input data selector/multiplexer

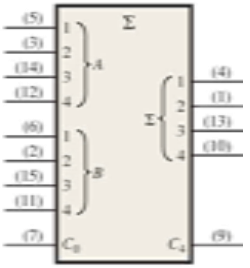


74HC154
1-of-16-line decoder

74HC157
Quad 2-input data selector/multiplexer

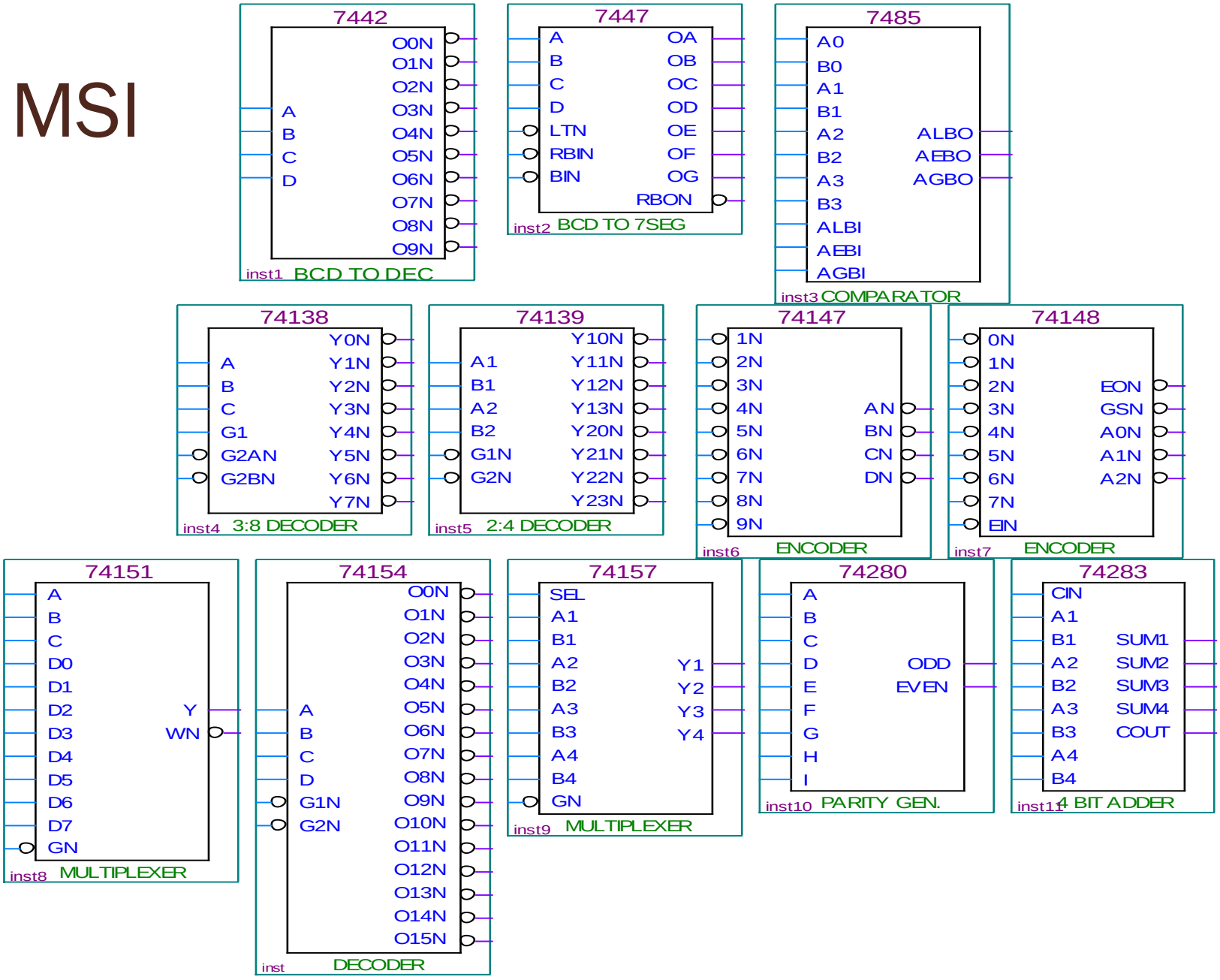


74LS280
9-bit parity generator/checker



74LS283
4-bit adder

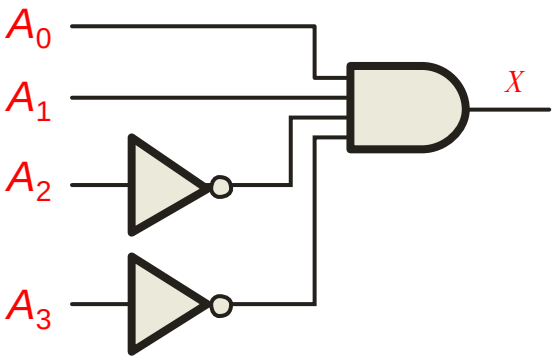
MSI


7442
A
B
C
D
O0N
O1N
O2N
O3N
O4N
O5N
O6N
O7N
O8N
O9N
inst1 BCD TO DEC
7447
A
B
C
D
LTN
RBIN
BIN
OA
OB
OC
OD
OE
OF
OG
RBON
inst2 BCD TO 7SEG
7485
A0
B0
A1
B1
A2
B2
A3
B3
ALBI
AEBI
AGBI
ALBO
AEBO
AGBO
inst3 COMPARATOR
74138
A
B
C
G1
G2AN
G2BN
Y0N
Y1N
Y2N
Y3N
Y4N
Y5N
Y6N
Y7N
inst4 3:8 DECODER
74139
A1
B1
A2
B2
G1N
G2N
Y10N
Y11N
Y12N
Y13N
Y20N
Y21N
Y22N
Y23N
inst5 2:4 DECODER
74147
1N
2N
3N
4N
5N
6N
7N
8N
9N
AN
BN
CN
DN
inst6 ENCODER
74148
0N
1N
2N
3N
4N
5N
6N
7N
EIN
EON
GSN
A0N
A1N
A2N
inst7 ENCODER
74151
A
B
C
D0
D1
D2
D3
D4
D5
D6
D7
GN
Y
WN
inst8 MULTIPLEXER
74154
A
B
C
D
G1N
G2N
O0N
O1N
O2N
O3N
O4N
O5N
O6N
O7N
O8N
O9N
O10N
O11N
O12N
O13N
O14N
O15N
inst DECODER
74157
SEL
A1
B1
A2
B2
A3
B3
A4
B4
GN
Y1
Y2
Y3
Y4
inst9 MULTIPLEXER
74280
A
B
C
D
E
F
G
H
I
ODD
EVEN
inst10 PARITY GEN.
74283
CIN
A1
B1
A2
B2
A3
B3
A4
B4
SUM1
SUM2
SUM3
SUM4
COUT
inst11 4 BIT ADDER

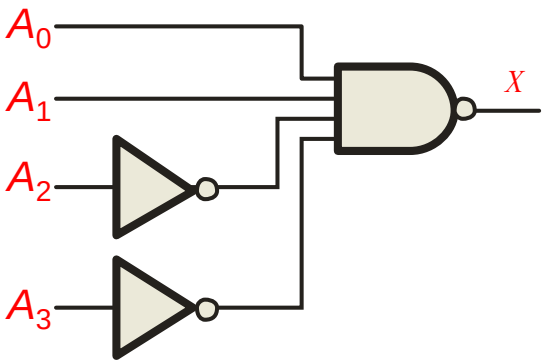
Simple Decoder

A **decoder** is a logic circuit that detects the presence of a specific combination of bits at its input.

Two simple decoders that **detect the presence** of the binary code 0011 are shown below. The first has an active HIGH output; the second has an active LOW output.



Active HIGH decoder for 0011

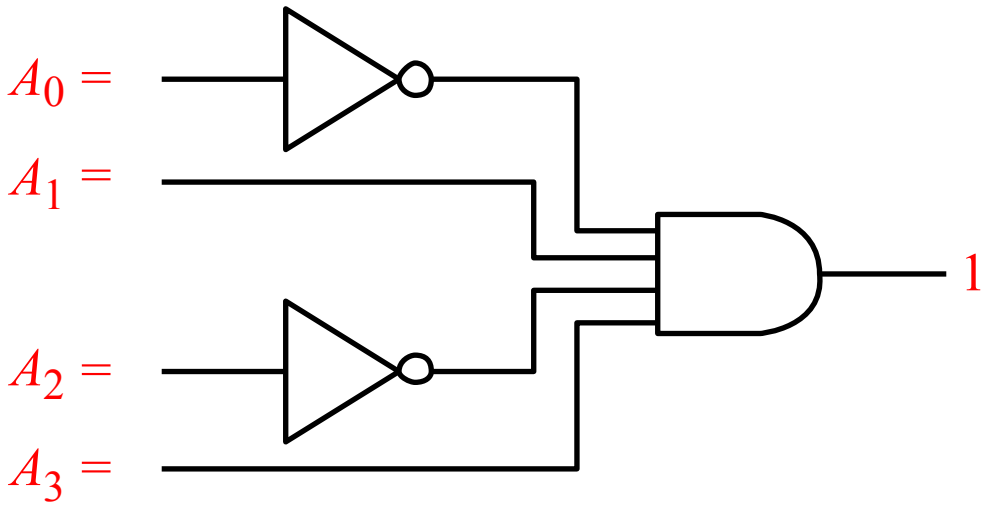


Active LOW decoder for 0011

(A_0 is the LSB and A_3 is the MSB)

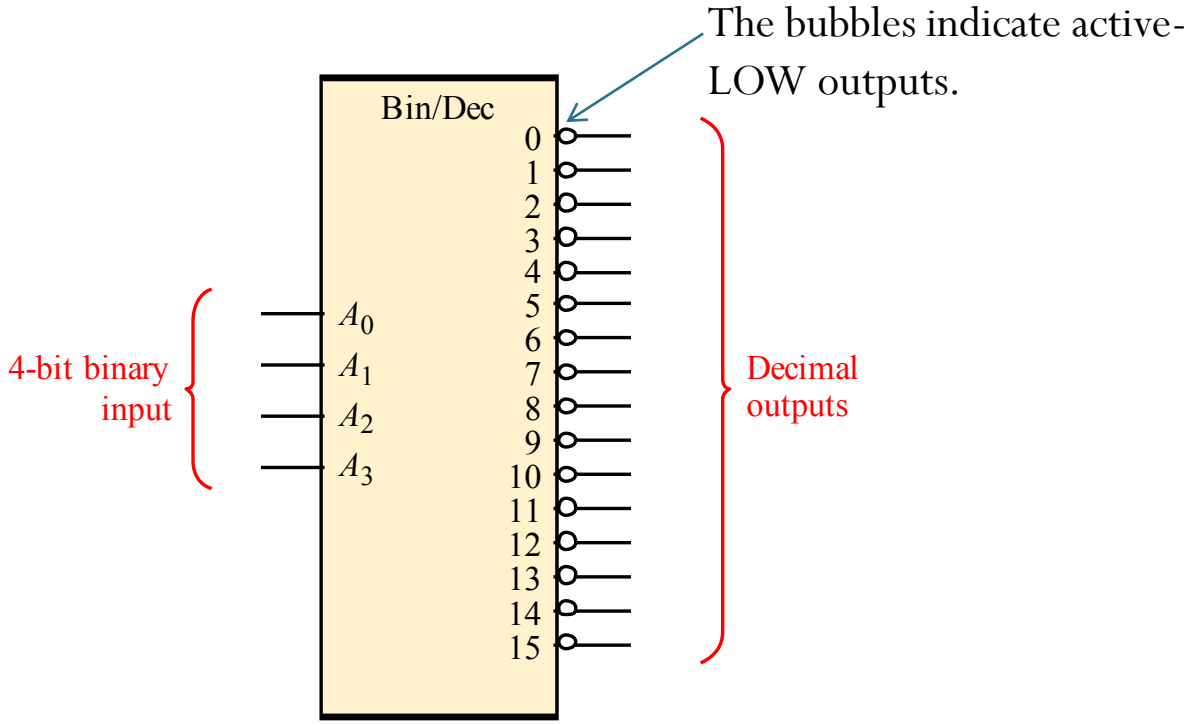
Exercise

Assume the output of the decoder shown below is a logic 1. What are the inputs to the decoder?



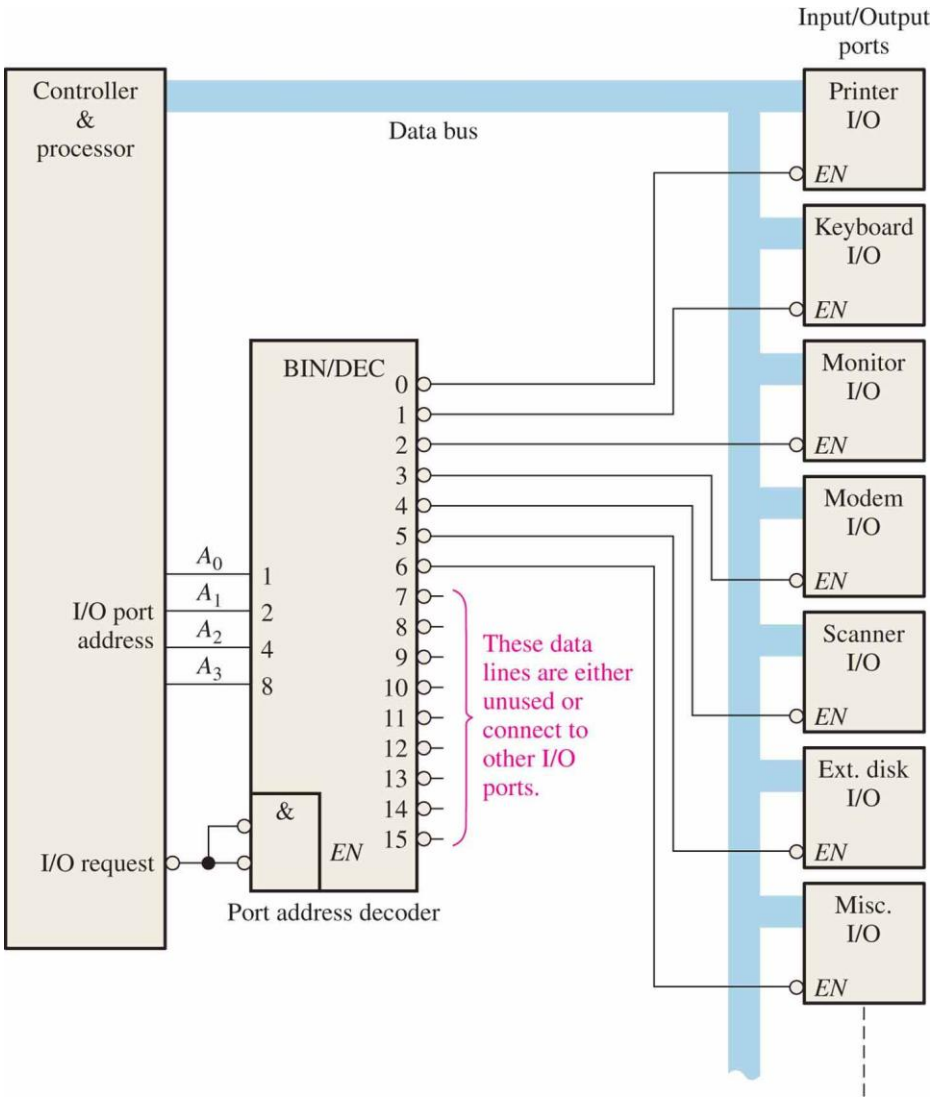
Binary-to-Decimal Decoder

The binary-to-decimal decoder shown here has 16 outputs – one for each combination of binary inputs.



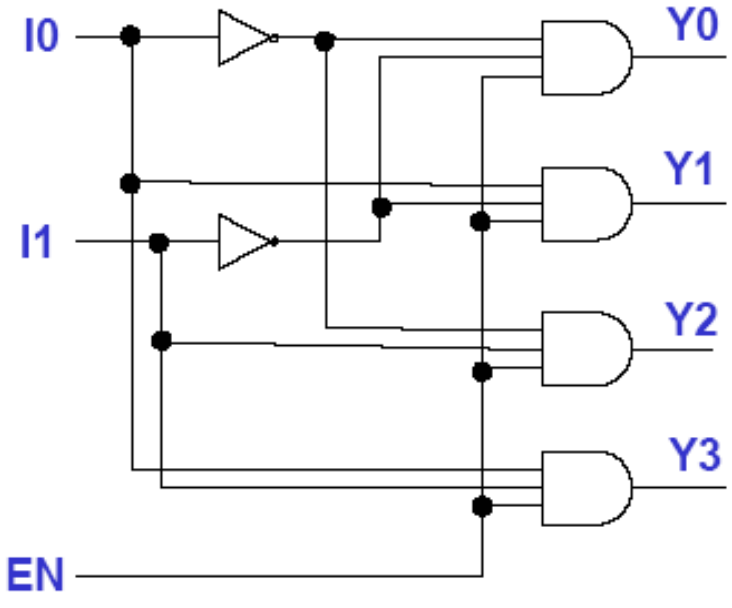
Application: Port Address Decoder

- Decoder can be used in computers for input/output selection.
- Computers communicate with peripherals by sending and/or receiving data through what is known as input/output (I/O) ports.
- A decoder can be used to select the I/O port so that data can be sent or received from a specific external device.



2:4 decoder

2-to-4 line decoder with enable input

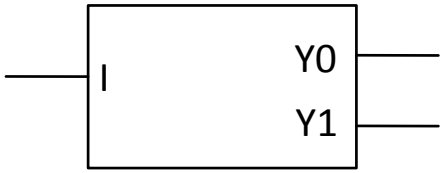


Inputs			Outputs			
EN	I1	I0	Y3	Y2	Y1	Y0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Exercise

Find the truth table of the 1-to-2 line decoder below.

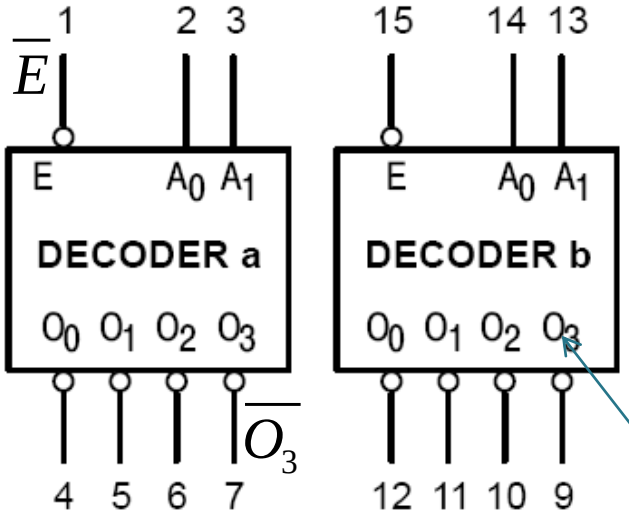
Then, implement the 1-to-2 line decoder.



74x139: Dual 2:4 Decoder

Most MSI decoders were originally designed with active-LOW output.

- Two independent 2:4 decoders
- The outputs and the enable (E) input are active-LOW.
- When *E* is HIGH all outputs are forced HIGH.

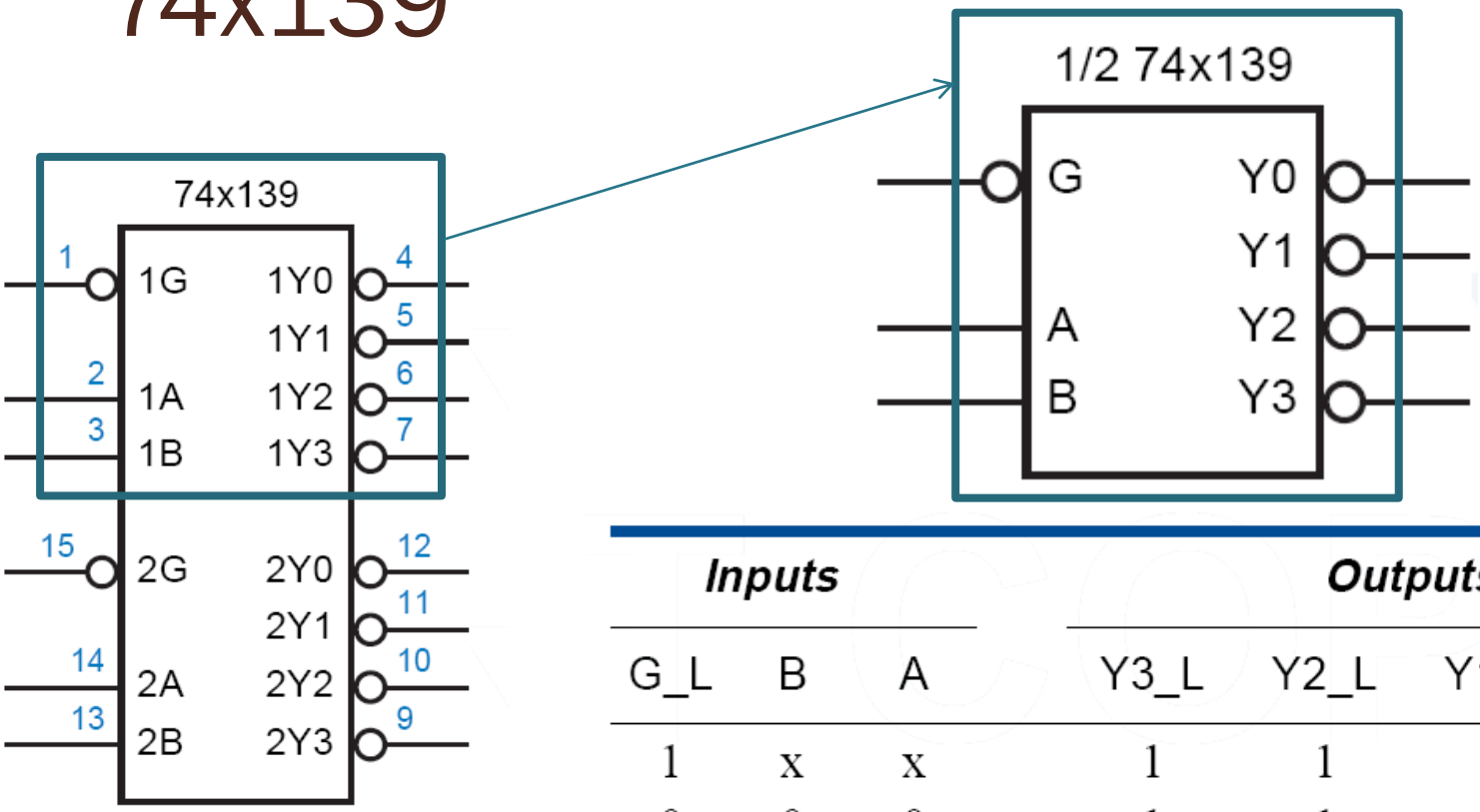


V_{CC} = PIN 16
GND = PIN 8

INPUTS			OUTPUTS			
E	A_0	A_1	O_0	O_1	O_2	O_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

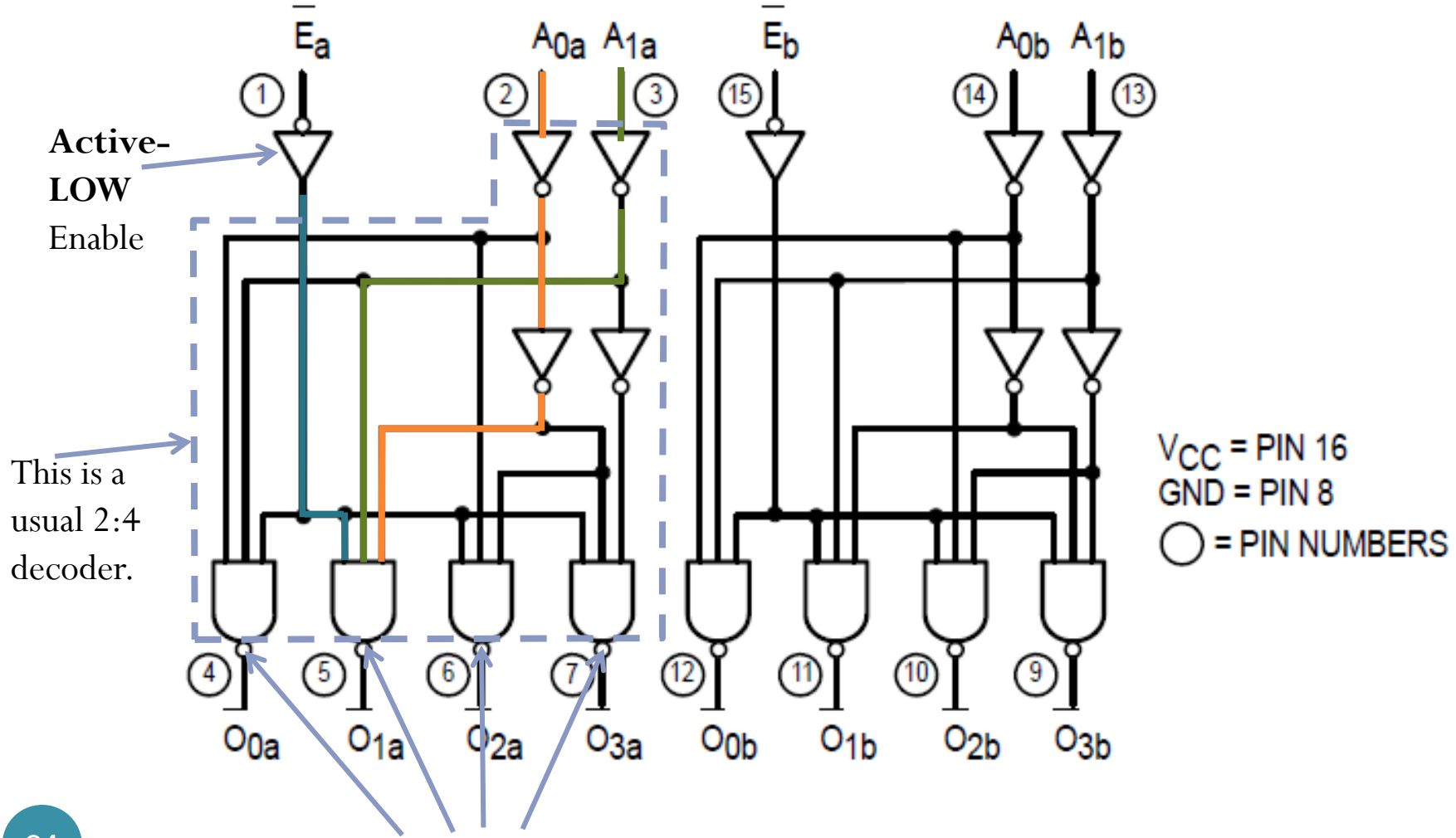
Notice that all of the signal names inside the symbol outline are active-HIGH, and that bubbles indicate active-LOW inputs and outputs.

74x139



Inputs			*Outputs*			
G_L	B	A	Y3_L	Y2_L	Y1_L	Y0_L
1	x	x	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

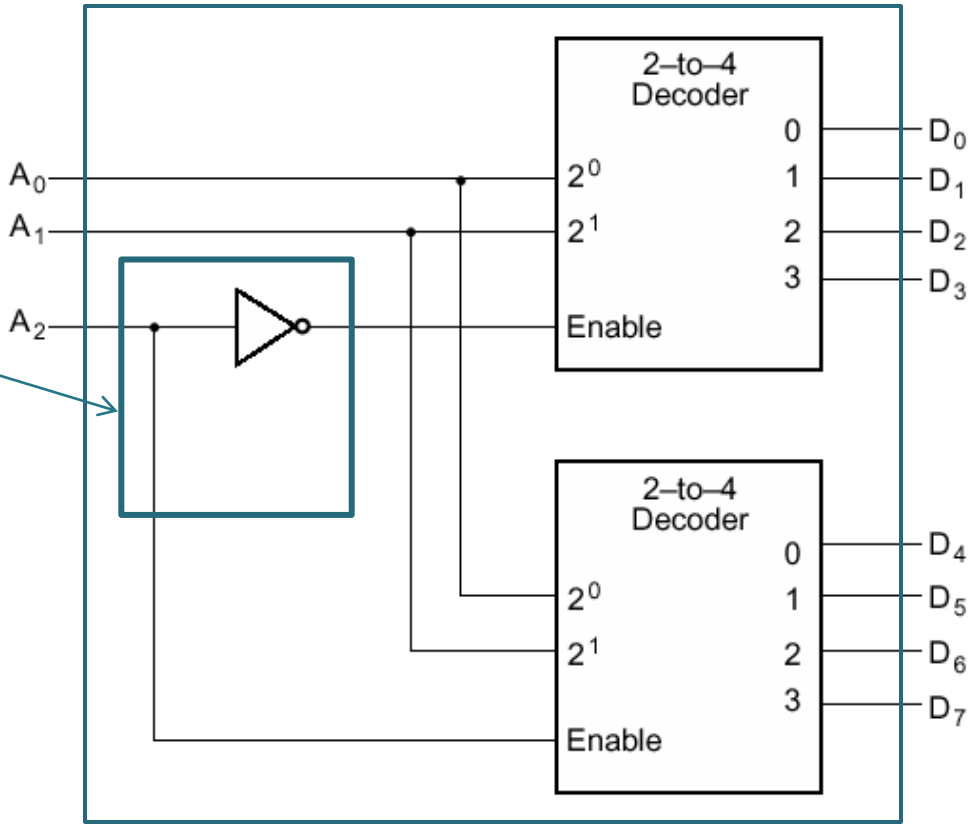
74x139: Logic diagram



Active-LOW output because NAND gates are used instead of AND gates

Example: Building a larger decoder

Construct a 3-to-8 decoder from two 2-to-4 decoders



Notice that this part is equivalent to a 1:2 decoder.

How can we add an active-HIGH enable input?

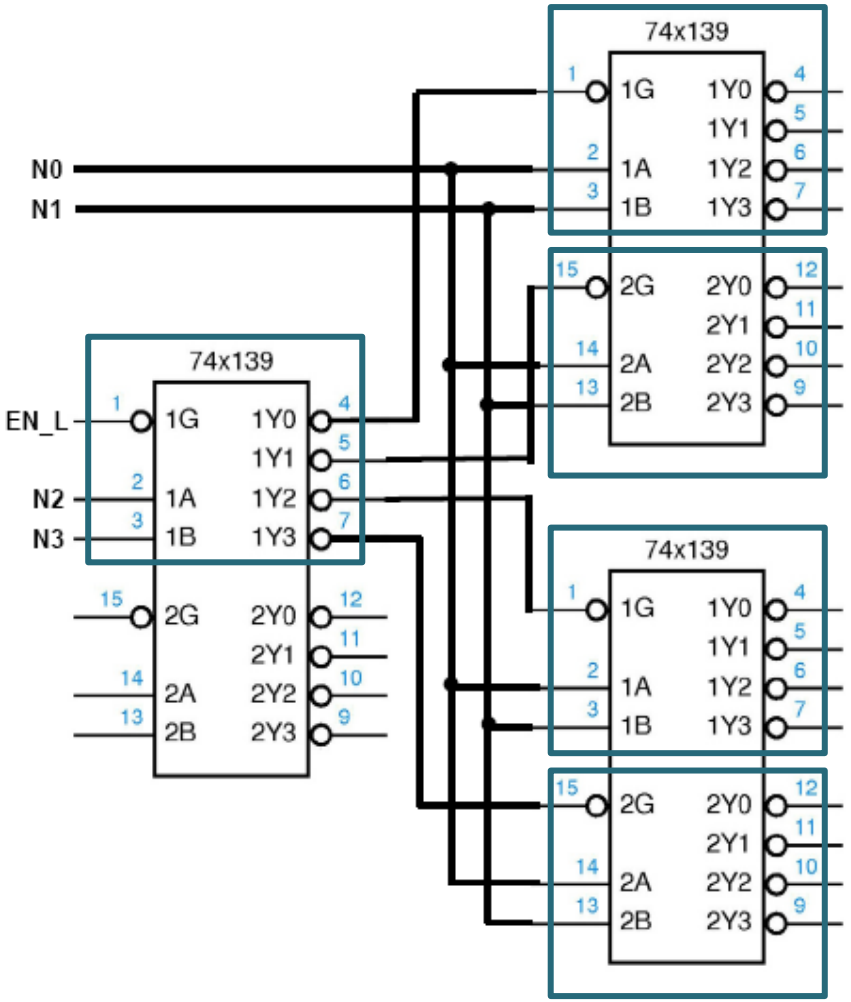
Low order bits (A_1, A_0) select within decoders. High order bit (A_2) controls which decoder is active.

Building larger decoder from smaller ones

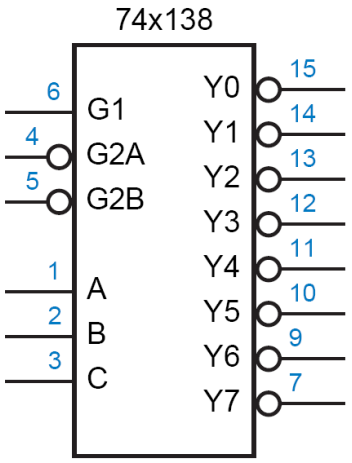
- To construct $(k+n)$-to-2^{n+k} decoders, can use
  1. 2^n of k-to-2^k decoders with enable input and
  2. one n-to-$2n$ decoders.
- The connections are:
  - For each of the k-to-2^k decoder with enable input,
    - all have k input
    - we put in $A_0 \ldots A_{k-1}$.
  - The enable line of the r^{th} decoder is connected to D_r of the n-to-2^n decoders.
  - The inputs of the n-to-2^n decoder get A_k to A_{n+k-1}.
- Basically, each k-to-2^k decoder works on the last k bits.
- We use the first n bit, via the n-to-2^n decoder, to select which one (and only one) of the k-to-2^k decoders will be enabled.

Example

Construct a 4:16 decoder with an active-LOW enable from three 2:4 decoders.



74x138: 3:8 Decoder

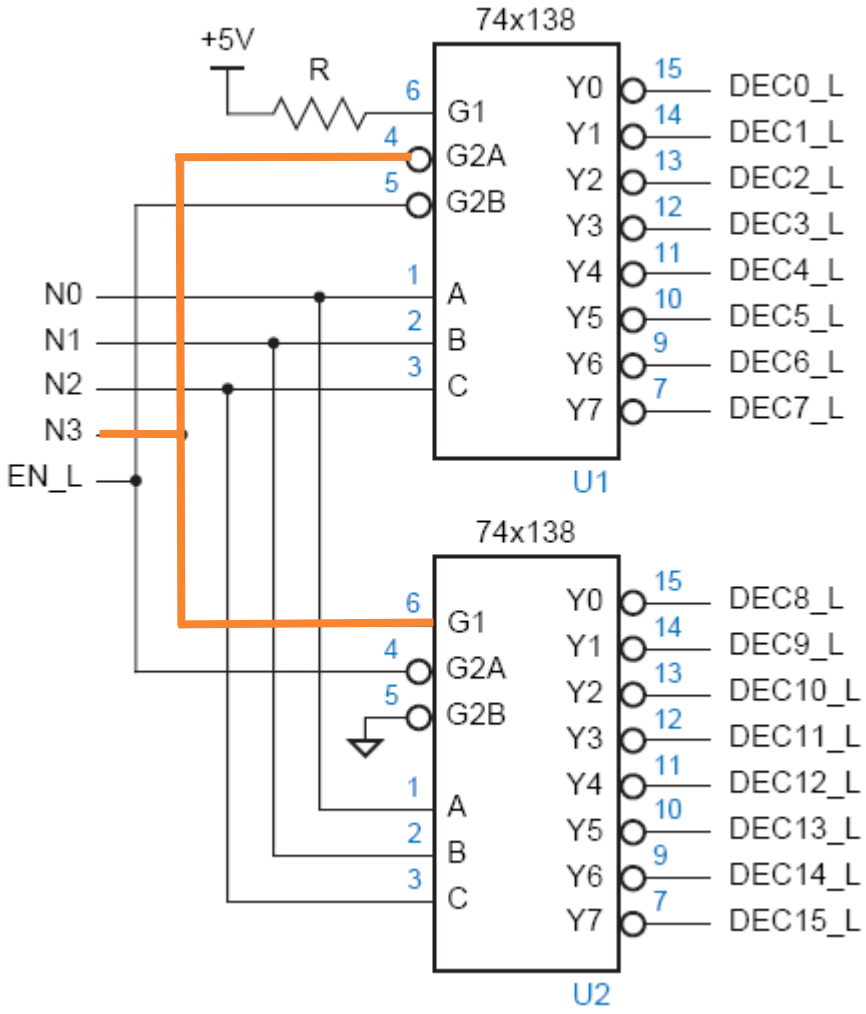


- Active-LOW outputs
- Three enable inputs.

Inputs						*Outputs*							
G1	G2A_L	G2B_L	C	B	A	Y7_L	Y6_L	Y5_L	Y4_L	Y3_L	Y2_L	Y1_L	Y0_L
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

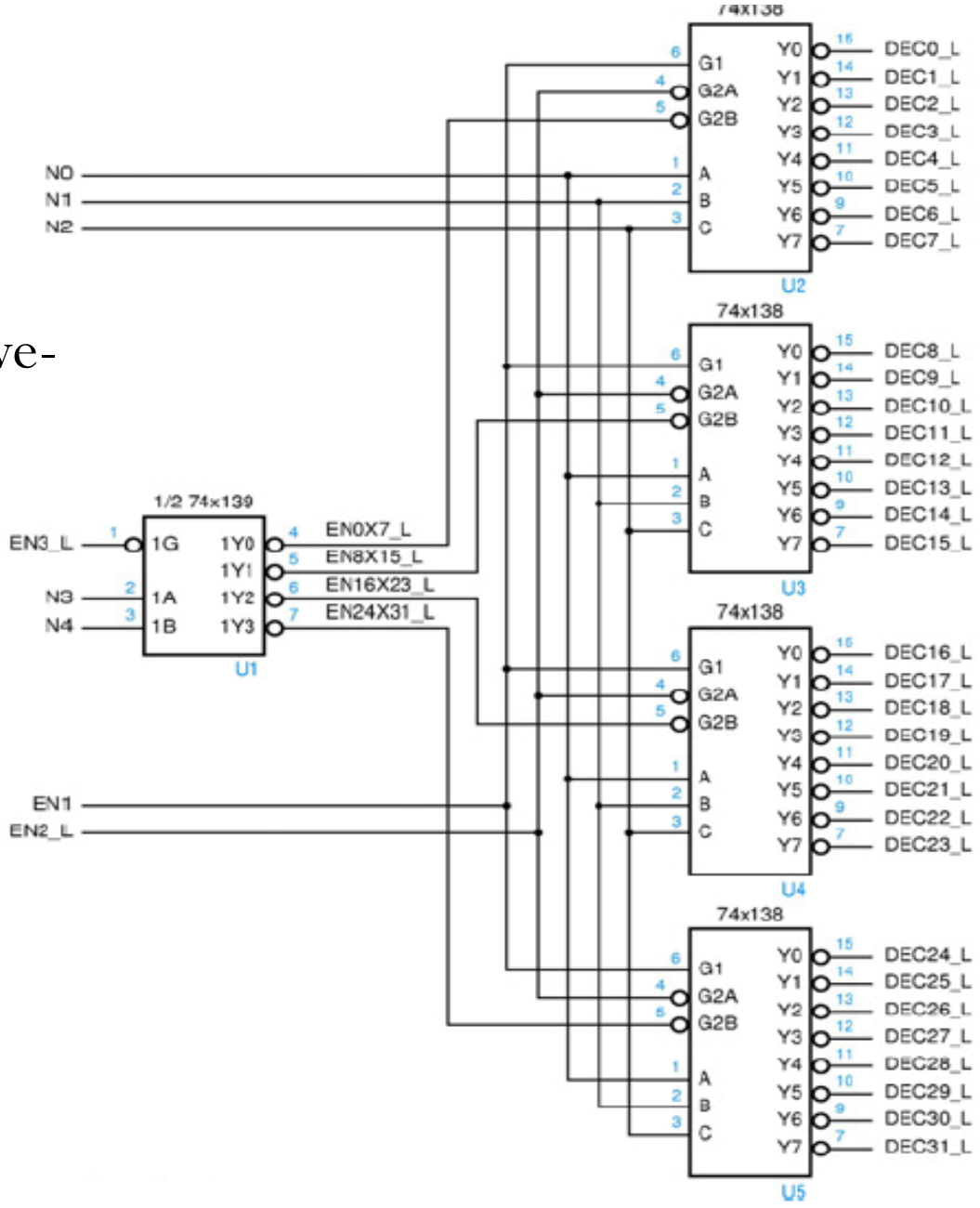
Example

Construct a 4:16 decoder with an active-LOW enable (EN) from two 74x138 decoder.

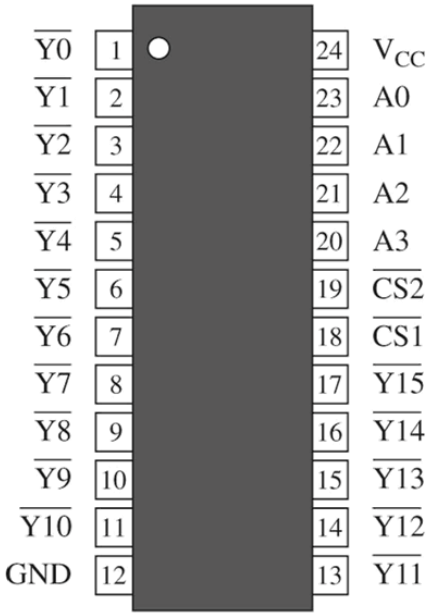


Example

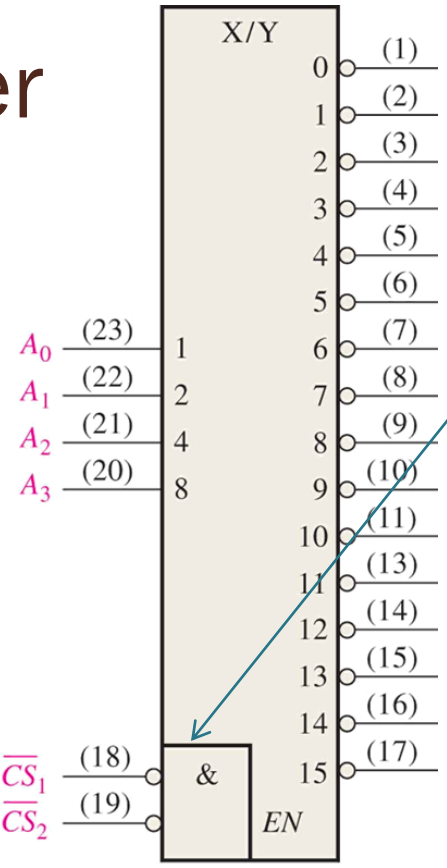
Construct a 5:32 decoder with two active-low enable and one active-high enable from four 74x138 and one 74x139.



74x154: 4:16 Decoder



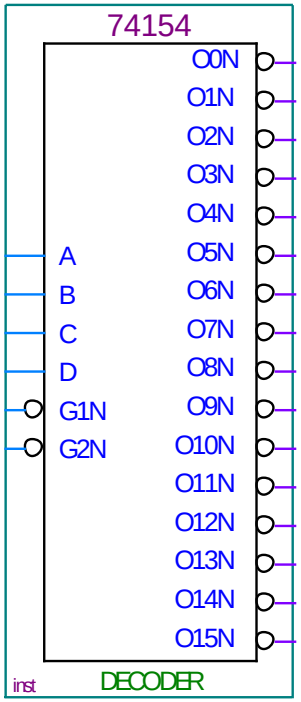
(a) Pin diagram



(b) Logic symbol

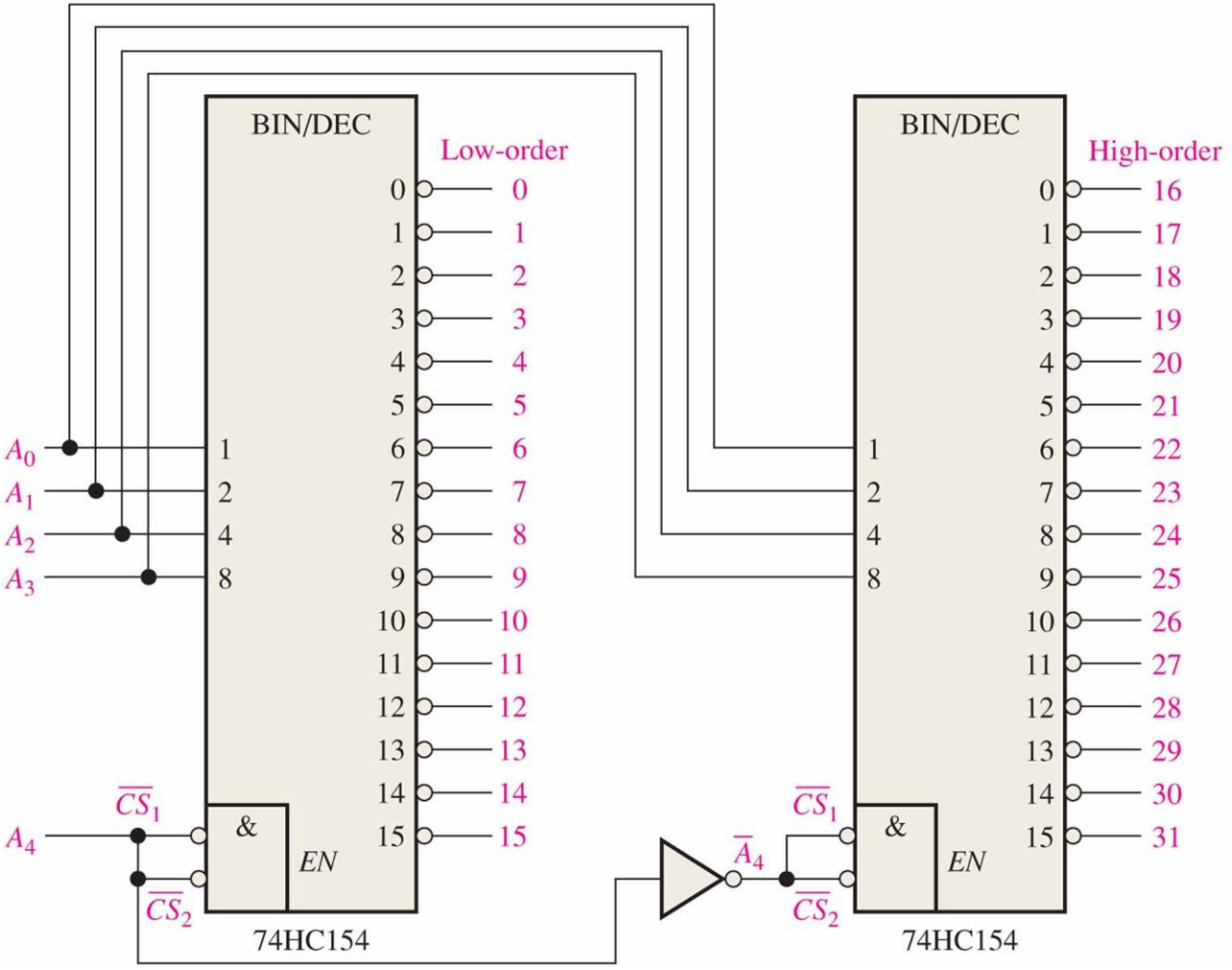
A LOW level on each chip select input is required to make the **enable** gate output (EN) HIGH.

Alternative logic symbol



Include two **active-LOW** chip select (CS) lines which must be at the active level to enable the outputs. These lines can be used to expand the decoder to larger inputs.

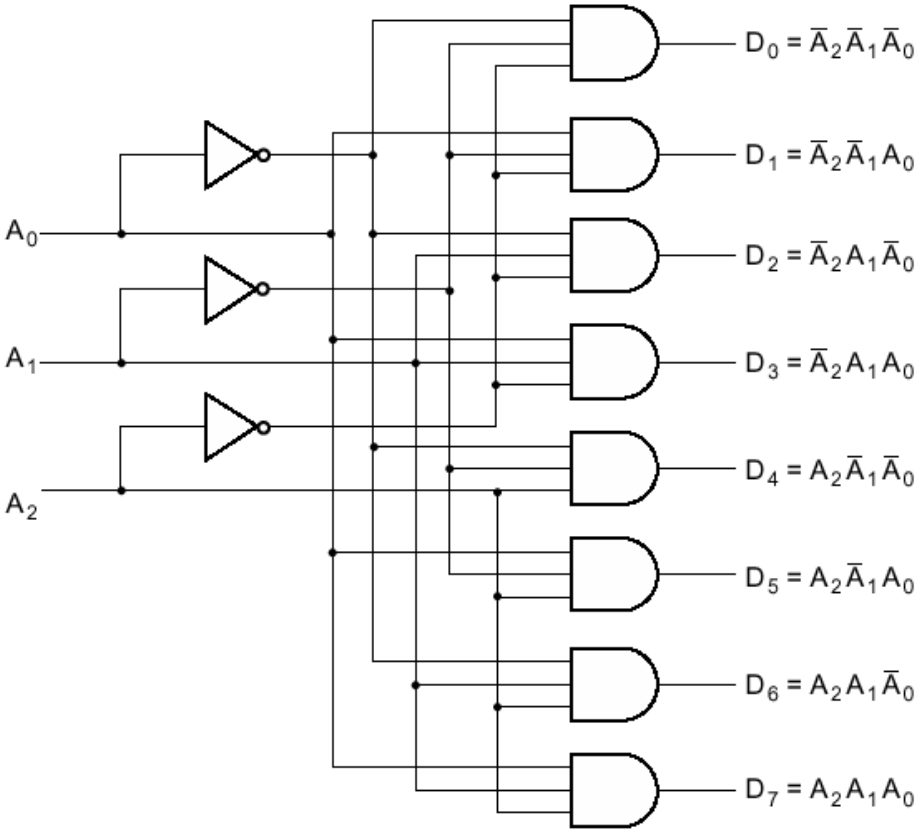
5:32 Decoder


BIN/DEC
Low-order
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
A_0
A_1
A_2
A_3
1
2
4
8
A_4
$\overline{CS}_1$
$\overline{CS}_2$
&
EN
74HC154
$\overline{A}_4$
BIN/DEC
High-order
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
74HC154

Decoder as general purpose logic

Any combinational circuit with n inputs and m outputs can be implemented with an n-to-2^n-line decoder and m OR gate

Observe that the 3:8 decoder generates all possible minterms.

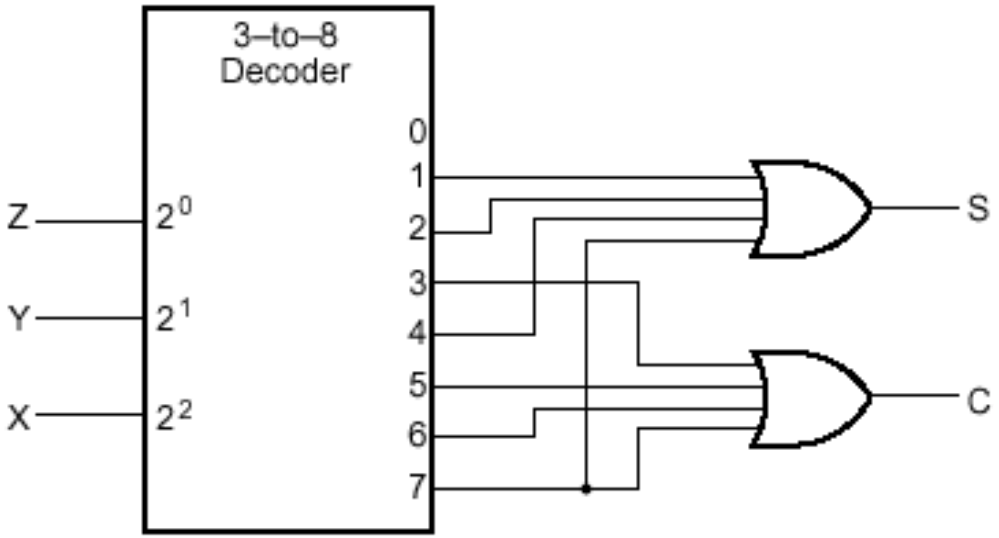


Example

Implement a full adder circuit with a decoder and OR gates

- $S = \sum_{X,Y,Z}(1,2,4,7)$
- $C = \sum_{X,Y,Z}(3,5,6,7)$

Inputs			Outputs	
X	*Y*	*Z*	*C*	*S*
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Other Decoders

In general, a decoder converts coded information, such as binary number, into non-coded form.

Later, (if time permitted) we will talk about other types of decoder.